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Statistical Variability and Reliability in Nanoscale FinFETs

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Abstract

A comprehensive full-scale 3D simulation study of statistical variability and reliability in emerging, scaled FinFETs on SOI substrate with gate-lengths of 20nm, 14nm and 10nm and low channel doping is presented. Excellent electrostatic integrity and resulting tolerance to low channel doping are perceived as the main FinFET advantages, resulting in a dramatic reduction of statistical variability due to random discrete dopants (RDD). It is found that line edge roughness (LER), metal gate granularity (MGG) and interface trapped charges (ITC) dominate the parameter fluctuations with different distribution features, while RDD may result in relatively rare but significant changes in the device characteristics.

Introduction

The statistical variability and reliability introduced by RDD, LER, MGG, and random ITC in nanoscale MOSFETs is becoming one of the major concerns for CMOS scaling and integration [1][2]. The 3D FinFET architecture, adopted by Intel in the upcoming 22nm generation, which tolerates low channel doping is, in part, a response to the requirement for reducing the statistical variability in nanoscale transistors [3][4]. This paper presents a comprehensive study of the statistical variability and reliability in scaled FinFETs featuring all relevant variability sources.

Devices and Simulation Methodology

The structure of the simulated FinFETs, fabricated on a SOI substrate, is schematically illustrated in Fig. 1. Relatively thin buried oxide (BOX) and high substrate doping are chosen to decouple drain-induced fringing fields and achieve optimal electrostatic integrity and short-channel effects [5]. The device parameters listed in Table 1 follow the ITRS 2010 recommendations, with slightly more conservative scaling of EOT and supply voltage. The design of the nominal devices with stress enhancement demonstrates excellent electrostatics and short channel effects (SCE) while achieving the desirable drive currents. The GSS ‘atomistic’ simulator GARAND is employed to investigate the statistical variability and reliability [6], illustrated by an example in Fig. 2. Variability sources including random discrete dopants (RDD), gate edge roughness (GER), fin edge roughness (FER), metal gate granularity (MGG), and interface trapped charge (ITC) are simulated, individually and in combination. The random

dopants are introduced based on the nominal local doping concentration. LER is obtained from Fourier synthesis with Gaussian autocorrelation, parameterised by correlation length (30nm) and root mean square (RMS) varied in the simulations [7]. TiN gate metal grains are assumed to have two different possible crystalline orientations with different workfunctions spanning 0.2V and having 40% and 60% probability of occurrence [1]. Ensembles of 1000 devices are used to minimise statistical error.

Statistical Variability

Full electrical transfer characteristics are simulated and the corresponding figures of merit are extracted and analysed. A combined variability case is demonstrated in Fig. 3 for a 10nm gate-length FinFET, illustrating the variation in transfer characteristics compared to the nominal design. The distributions of threshold-voltage (V_T) in the three FinFET designs show that the overall V_T variability is dramatically reduced compared to planar bulk MOSFETs [1][2], but the new variability source, fin-edge roughness, contributes considerable variability. Another dominant source is MGG, while RDD effects are significantly suppressed (Fig. 4) due to the lack of channel doping. The V_T spread increases with the gate area reduction for the scaled FinFET.

The normal Q-Q test on the V_T distribution due to RDD in Fig. 5(a) shows that it closely follows a Gaussian distribution. The additional simulations show that source/drain resistance variation due to doping fluctuations dominates the RDD variability due to the absence of channel doping. However, a single dopant rarely but possibly located in the channel can dramatically reshape the distribution tails. Observed in two extreme cases of the 14nm FinFET in Fig. 5(b), one donor in the channel can pull down the left tail of the distribution and one acceptor can elevate the right tail. The LER effects are shown in Figures 6 and 7. Compared to that due to FER, GER produces a skewed V_T distribution with a prolonged left tail, especially in the 10nm FinFET due to stronger SCE. However, for thin fin width, the FER can also produce a skewed distribution. Different asymmetrical sensitivity of V_T to the changes in gate-length and fin-width, as shown in Fig. 8, is the reason for the observed behaviour. In addition, the threshold-voltage is more sensitive to fin-width variation compared to gate-length, causing larger FER variability than GER. The asymmetrical distribution in 10nm FinFETs due to FER is caused by the dramatically reduced current density inside the channel due to quantum

confinement, demonstrated in Fig. 9. TiN MGG can cause a bounded, dual-peaked V_T distribution (Fig. 10) when metal-grain size is comparable to gate dimensions although it approximates to a Gaussian distribution with small metal grain sizes, as shown in Fig. 11. In general, the V_T variability increases with the reduction in size of FinFETs while the MGG and FER are dominant sources in all three FinFETs (Fig. 12). The standard deviation of threshold-voltage can reach up to 31.5mV, 41.5mV and 51.3mV for 20nm, 14nm and 10nm gate-length FinFETs with all variability sources combined. This overall variation of device performance depends on the variability-source parameters. From Fig. 13 σV_T is linearly proportional to the RMS (Δ) of the LER. Combined with the observations from Fig. 8, LER-induced variability is proportional to LER magnitude and sensitivity. However, similar to MGG in bulk transistors, the linear proportionality does not hold true with large metal grains.

The on-current (I_{ON}) variation has different distribution features in Fig. 14. FER introduces the largest I_{ON} variability since FER does not just affect the channel but also the source/drain resistances, while RDD together with MGG also contribute considerably. Meanwhile MGG has the strongest correlation between I_{ON} and V_T variations, but the I_{ON} with combined sources stays less correlated with V_T , which means I_{ON} is also statistically important (Table 2). The drain-induced barrier lowering (DIBL) correlations with V_T due to two dominant variability sources, FER and MGG, are different (Fig. 15). The DIBL has strong negative correlations with both linear and saturation threshold voltages in the presence of FER, since fin-width thinning can lead to higher threshold-voltage (both for saturation and linear) and better short-channel effects. In the presence of MGG, the drain field lowers the drain-end channel barrier, which is subject to surface potential variation, and therefore DIBL exhibits large variation.

Statistical Reliability

Random trapped charges at the gate oxide/fin interface in FinFETs subjected to NBTI/PBTI degradation demonstrate the statistical aspect of reliability. As an example showing trapped charges in the 3D FinFET in Fig. 16(a), traps can significantly reduce the current nearby, and even block the current in the thin fin when two or more traps are coincidentally located on opposite sides, as demonstrated in Fig. 16(b). The electron and current distributions inside the fin, due to the confining oxide barrier on all four sides, are centralised away from the interfaces. A fixed interface trap charge locally lowers the electrostatic potential, reducing the electron density nearby, further confining the carriers in the channel. Fig. 17 shows the distribution of V_T -shift due to extra traps. For any given device, V_T increases with a magnitude depending on the number and location of the trapped charges. With nominal trap density $1 \times 10^{11} \text{ cm}^{-2}$ in the 20nm FinFET there is, on average, only one trapped charge, which can lead to V_T random telegraph signal (RTS) of

several millivolts. However, a large V_T -shift in the distribution tail is observed, demonstrating that multi-trapping RTS occurs [8]. A simple model, $\Delta V_T = qN_{it}/C_{ox}$, assumes that interface charges (and/or oxide charges close to the oxide/fin interface) cause a flat-band voltage change. Due to multi-gate control the average V_T shift is less than the modelled shift (Fig. 18). The average shift is linearly proportional to the average trap density as expected, but the magnitude is reduced because of the enhanced capacitance. The location of individual traps, for the same number of traps, can affect the overall V_T variability (Fig 19). This variation is especially prominent if the number of traps is around the average. Combining two facts from Fig. 18 and 19, σV_T more or less follows the modelled $q t_{ox} \sqrt{N_{it}} / (\epsilon_{ox} \sqrt{WL})$ assuming the number of traps follows a Poisson distribution [9] in Fig. 20.

Conclusions

Full-scale statistical simulation and analysis of intrinsic parameter fluctuation in 3D FinFETs is presented. FER and MGG are dominant V_T variability sources in nanoscale FinFETs while LER may skew the variability, and FER could lead to the largest drive-current variability. Other figures of merit and their correlations are analysed together. ITC can considerably shift the characteristics, introducing an additional statistical aspect of threshold-voltage reliability.

Acknowledgements

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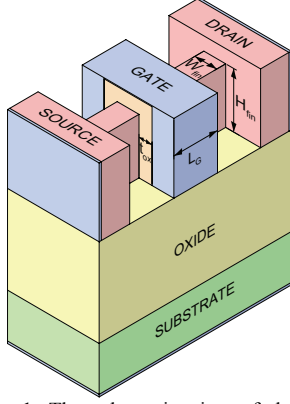


Fig. 1: The schematic view of the 3D SOI FinFET in this study. BOX is 20nm thick, and substrate doping is $5 \times 10^{18} \text{cm}^{-3}$.

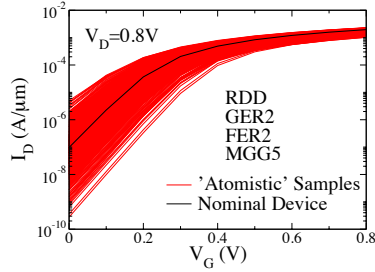


Fig. 3: Full electrical transfer characteristics simulation of 10nm gate-length FinFETs, including random discrete dopants (RDD), gate edge roughness (GER) with $3\Delta=2\text{nm}$, fin edge roughness (FER) with $3\Delta=2\text{nm}$, and metal gate granularity (MGG) with average grain diameter of 5nm.

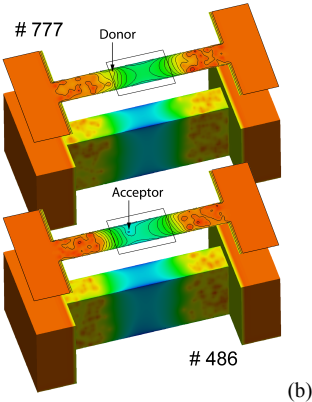
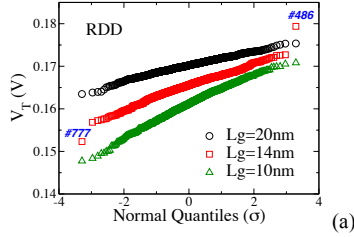


Fig. 5: (a) The normal Q-Q test on V_T distributions due to RDD in 3 FinFETs. (b) Two rare extreme cases at the ends of the distribution tails of the 14nm FinFET with a single dopant in the channel.

Table 1: The FinFET parameters

Node (nm)	22	16	11
L_g (nm)	20	14	10
EOT (nm)	0.83	0.7	0.585
W_{fin} (nm)	10	7	5
H_{fin} (nm)	25	17.5	12.5
N_{sd} (cm^{-3})	$3E20$	$3E20$	$3E20$
N_{ch} (cm^{-3})	$1E15$	$1E15$	$1E15$
V_{dd} (V)	1	0.9	0.8
I_{off} (nA/ μm)	97	97	97
I_{dsat} ($\mu\text{A}/\mu\text{m}$)	1411	1719	1958
SS (mV/dec)	76.8	75.1	73.2
DIBL (mV/V)	46.7	46.8	47.0

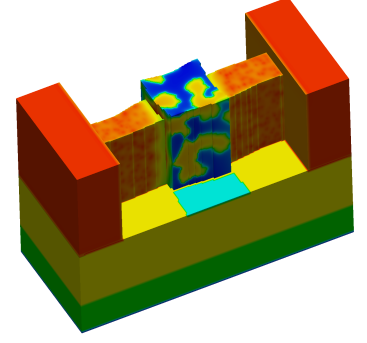


Fig. 2: Full-scale 3D statistical simulations of FinFETs, showing the electron density in the fin and potential on the gate. It is easily seen that doping fluctuations, fin-edge and gate-edge roughness, and gate workfunction fluctuation are occurring in concert.

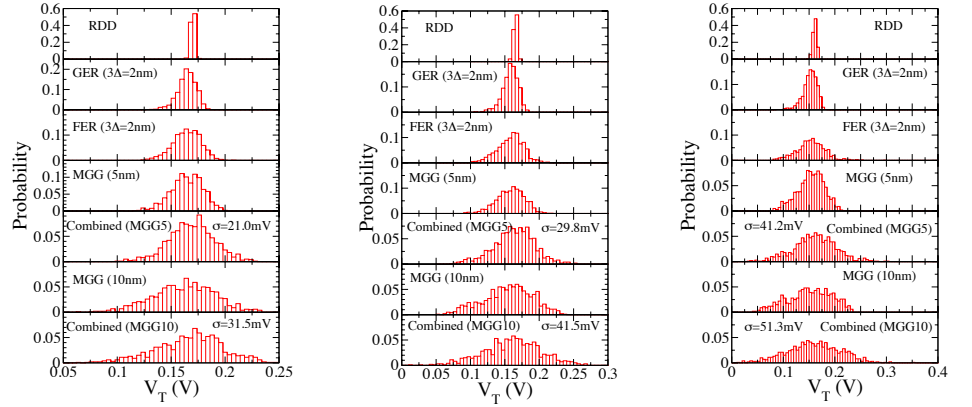


Fig. 4: The distributions of threshold-voltages (V_T) due to different variability sources in three generations of FinFETs with gate lengths of 20nm (left), 14nm (middle) and 10nm (right).

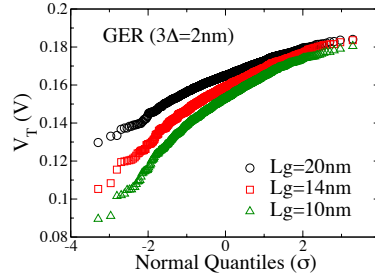


Fig. 6: The Q-Q test on V_T distribution due to gate-edge roughness. It is seen that the smaller FinFET has more strongly skewed tails. It shows that GER causes a prolonged left tail in the V_T distribution.

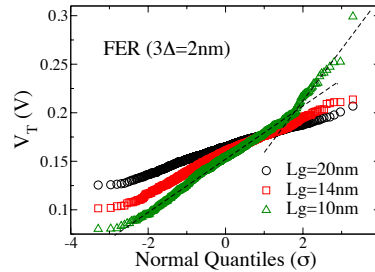


Fig. 7: The Q-Q test on V_T distribution due to fin-edge roughness. The distribution of 10nm FinFET deviates from the normal distribution on the right side.

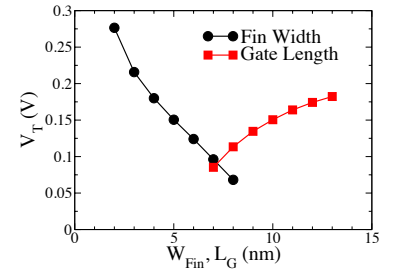


Fig. 8: The sat. V_T dependence on fin-width and gate-length for the 10nm device. It is found that the sensitivities to these two geometrical parameters are different on both sides

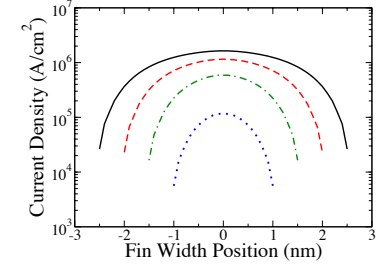


Fig. 9: The current density inside the channel of the 10nm gate-length FinFET with fin width of 5nm, 4nm, 3nm and 2nm. $V_d=0.05\text{V}$, $V_g=0.2\text{V}$.

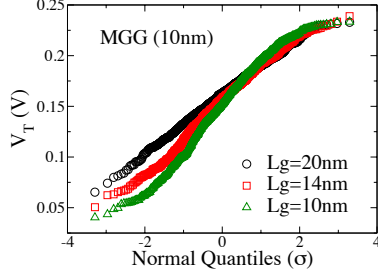


Fig. 10: The Q-Q test on V_T distribution due to MGG with average grain-diameter 10nm. It is seen that the small FinFET has bounded tails.

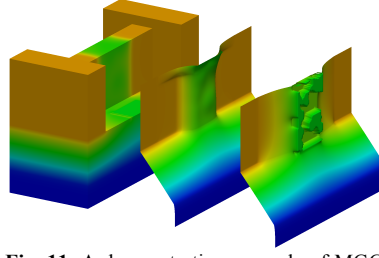


Fig. 11: A demonstrative example of MGG. The right slice demonstrates workfunction variation effects on gate potential, and middle slice shows corresponding surface potential variation.

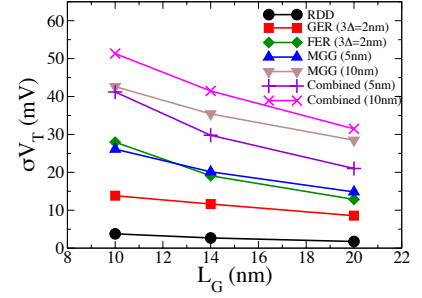


Fig. 12: The gate-length dependence of σV_T for different variability sources.

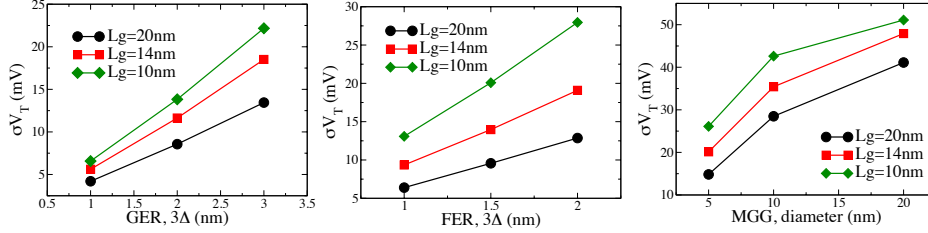


Fig. 13: σV_T dependence of V_T variability respectively on GER root mean square (RMS, Δ) (left), FER RMS (middle). The linear proportionality dependence is observed for small RMS. The σV_T dependence of V_T variability on MGG average grain diameter (right graph) shows it does not increase with grain size linearly due to the bounded nature of the distribution between the two possible workfunctions.

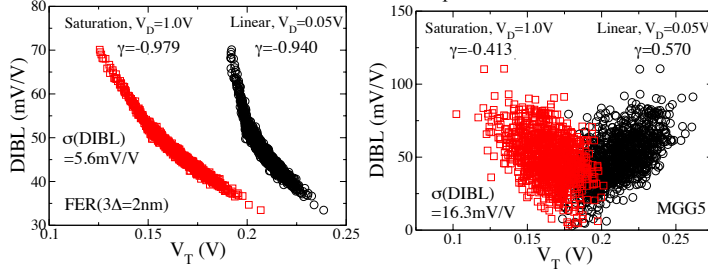
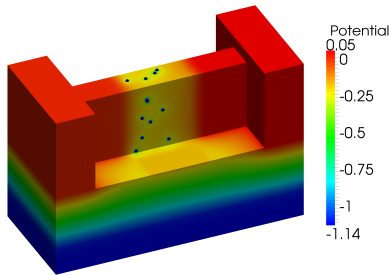


Fig. 15: The DIBL variation due to major variability sources FER (left) and MGG (right) in the 20nm gate-length FinFET. DIBL has stronger correlations with V_T due to FER than due to MGG, but less variation than due to MGG.

Lg (nm)	20	14	10
RDD	-0.795	-0.766	-0.782
GER2	-0.876	-0.798	-0.706
FER2	-0.890	-0.902	-0.943
MGG5	-0.935	-0.945	-0.960
MGG10	-0.968	-0.970	-0.981
Combined5	-0.739	-0.746	-0.785
Combined10	-0.812	-0.799	-0.830



(a) **Fig. 17:** Q-Q plot for V_T shift due to random interface traps in stressed devices without other variability sources.

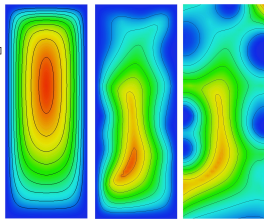
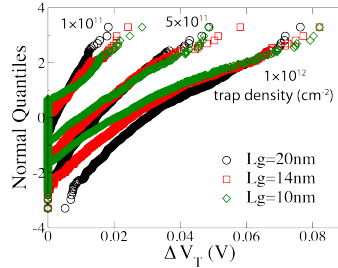


Fig. 16: Random interface traps in a 20nm gate-length FinFET are shown in (a), and a cross-section view of current density (b) for cases without traps (left), with six traps (middle) and with six traps but simulated without quantum corrections (right). $V_g=0.2V$.



(a) **Fig. 17:** Q-Q plot for V_T shift due to random interface traps in stressed devices without other variability sources.

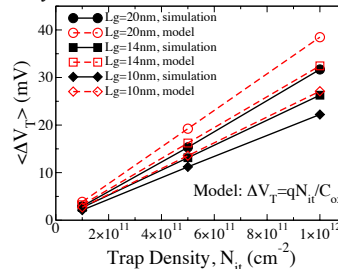


Fig. 18: Average V_T shift due to trapped charges. It is less than that from the analytical model.

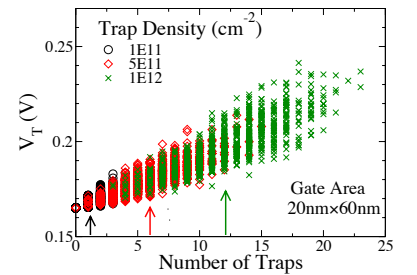


Fig. 19: Placement of random traps contributes to overall variability.

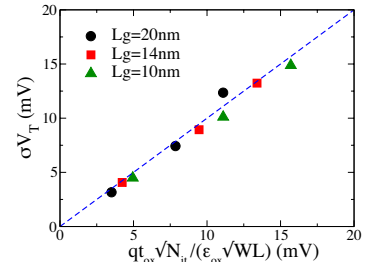


Fig. 20: The σV_T due to random interface traps, testing an analytic model.